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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of		TI-30481
	Gary L. Swoboda, et al.	Art Unit: 2128
Serial No.:	09/943,599	Examiner: Akash Saxena
Filed:	August 30, 2001	Conf. No.: 2479
For:	Correlating On-Chip Data Processor Trace Information for Export	

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NAME OF INVENTOR(S): Gary L. Swoboda, et al.	RECEIPT DATE & SERIAL NO.: **Serial No.: 09/943,599** **Filing Date:** August 30, 2001
TITLE OF INVENTION: Correlating On-Chip Data Processor Trace Information for Export	
TI FILE NO.: **TI-30481** / DEPOSIT ACCT. NO.: **20-0668**	
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TI-30481
Docket No.

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Robin E. Barnum

In re Application of

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Conf. No: 2479

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Transmitted herewith is an Appeal Brief in the above-identified application.

Please charge the $500.00 fee for filing the Brief to Texas Instruments Incorporated, Deposit Account No. 20-0668.

Charge any additional fees, or credit overpayment to Texas Instruments Incorporated, Deposit Account No. 20-0668.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Swoboda et al
Serial No.: 09/943,599
Filed: August 30, 2001
For: CORRELATING ON-CHIP DATA PROCESSOR TRACE INFORMATION FOR EXPORT

Art Unit: 2128
Examiner: Akash Saxena
Docket: TI-30481

Appeal Brief under 37 C.F.R. §41.37

Board of Patent Appeals and Interferences
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Robin E. Barnum

Dear Sir:

This is Appellant's Appeal Brief filed pursuant to 37 C.F.R. §41.37 and the Notice of Appeal filed January 11, 2006.

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Real Party in Interest

The real party in interest in this application is Texas Instruments Incorporated, a corporation of Delaware with its principle place of business in Dallas, Texas. An assignment to Texas Instruments Incorporated is recorded at reel 011864 and frames 0744 to 0745 in U.S. Patent Application Serial No. 09/798,561, the parent application of this divisional application, now U.S. Patent No. 6,985,848.

Related Appeals and Interferences

There are no appeals of interferences related to this appeal in this application.

Status of the Claims

Claims 1, 4, 5, 13, 14, 16, 23, 24 and 27 to 30 are rejected and subject to this appeal. No claims are allowed. Claims 2, 3, 6 to 12, 14, 17 to 22, 25 and 26 are canceled.

Status of Amendments Filed After Final Rejection

No amendments to the claims were proposed following the FINAL REJECTION of September 9, 2005.

Summary of Claimed Subject Matter

This invention is a method of providing data processor emulation information that can be practiced in an apparatus such as a integrated circuit and a data processing system. The method provides a program counter trace stream (Figure 8, "PC TRACE PACKET STREAM" output of PC TRACNE PACKET GENERATOR 82; page 14, line 10) of program counter values (Figure 8 "PC") used by a data processor (14). The method inserts a synchronization marker (Figure 6 "010 SYNC POINT PERIODICALLY GENERATED, Figure 7, page 25, line 8 to page 26, line 3) into the program counter trace stream. The method

provides trace information identifying the program counter value by expressing the corresponding program counter value as an offset from the synchronization marker (page 8, lines 8 to 11; page 28, liens 3 and 7; page 30, line 18 to page 31, line 1; Figure 9 "OFFSET BITS 7-0 (8 BITS)" and "OFFSET BITS 15-8 (8 BITS)(OPTIONAL)"). The method detects occurrences of program counter loads (page 30, lines 14 to 15; Figure 11 "PC LOAD" signal to "INC" input of counter 112) and identifies the program counter value by counting program counter loads)page 30, lines 30 to page 31, line 1) by maintaining a running count (112) of a number of program counter loads that have occurred since insertion of the synchronization marker (page 30, lines 16 to 18).

Grounds for Rejection to be Reviewed on Appeal

(1) Claims 1, 4 and 5 were rejected under 35 U.S.C. 102(e) as anticipated by Mann, U.S. Patent No 6,009,270.

(2) Claims 13, 15 and 16 were rejected under 35 U.S.C. 103(a) as made obvious by the combination of Sites et al U.S. Patent No. 5,764,885, and Mann U.S. Patent No 6,009,270.

(3) Claims 23, 24 and 27 to 30 were rejected under 35 U.S.C. 103(a) as made obvious by the combination of Sites et al U.S. Patent No. 5,764,885, Mann U.S. Patent No 6,009,270 and Edwards U.S. Patent No. 6,732,307.

Arguments

(1) Claims 1, 4 and 5 were rejected under 35 U.S.C. 102(e) as anticipated by Mann U.S. Patent No 6,009,270.

Claim 1 recites subject matter not anticipated by Mann. Claim 1 recites "identifying a program counter value" and "expressing said corresponding program counter value as an offset which indicates a number of program counter values in the program counter trace stream by which said corresponding program counter value is offset from said synchronization marker in said program counter trace stream." The FINAL REJECTION incorporates the arguments of the OFFICE ACTION of March 22, 2005 which cites Mann at column 13, lines 56 to 62 as teaching "that branching causes disruption in the flow and non-data dependent branching...can be represented in a form of an offset indicating whether the branch was taken or not." Mann states at column 13, lines 56 to 62:

> "Preferably, only instructions which disrupt the instruction flow are reported; and further, only those where the target address is in some way data dependent. For example, such 'disrupting' events include call instructions or unconditional branch instructions in which the target address is provided from a data register or other memory location such as a stack."

This portion of Mann fails to teach the claimed "offset which indicates a number of program counter values in the program counter trace stream by which said corresponding program counter value is offset from said synchronization marker." The claimed synchronization marker is not mentioned in this portion of Mann. There is no mention of reporting the program counter value based upon "a number of program counter values" difference with such a synchronization marker. The OFFICE ACTION of March 22, 2005 cites Mann at column 14, lines 7 to 16 as teaching "This offset

information is presented in form of a trace entry." Mann states at column 14, lines 7 to 16:

> "FIG. 6A illustrates an exemplary format for reporting conditional branch events. In the disclosed embodiment of the invention, the outcome of up to 15 branch events can be grouped into a single trace entry. The 16-bit TDATA field (or 'BFIELD') contains 1-bit branch outcome trace entries, and is labeled as a TCODE=0001 entry. The TDATA field is initially cleared except for the left most bit, which is set to 1. As each new conditional branch is encountered, a new one bit entry is added on the left and any other entries are shifted to the right by one bit."

The "exemplary format for reporting conditional branch events" includes a bit for each such conditional branch indicating it was taken or not taken. This portion of Mann likewise fails to teach the claimed synchronization marker, or the claimed offset. The OFFICE ACTION of March 22, 2005 cites Mann at column 15, lines 8 to 13 and 53 to 56 as teaching "from which new target value can be reconstructed." Mann states at column 15, lines 8 to 15 (including the portion cited in the FINAL REJECTION):

> "When processing a trace stream in accordance with the invention, trace address values are combined with a segment base address to determine an instruction's linear address. The base address, as well as the default data operand size (32 or 16-bit mode), are subject to change. As a result, the TCODE=0011 and 0111 entries are configured to provide the information necessary to accurately reconstruct instruction flow."

This portion of Mann teaches that the trace address values are an offset that is combined with a segment base address "to determine an instruction's linear address." This portion of Mann teaches providing "the information necessary to accurately reconstruct instruction flow." Thus Mann also teaches that a change in segment base address is communicated as part of the trace stream. This

portion of Mann includes no teaching that a synchronization marker is the same as the segment base address. For example, Mann teaches providing a new synchronization marker following a taken conditional branch whose target address is data in a register at column 3, lines 5 to 7. However, Mann fails to teach that the trace address values following such a synchronization marker are offset from the synchronization marker value. Instead, Mann teaches that the trace address values are offset from the prior and still unchanged segment base address. Accordingly, claim 1 is not anticipated by Mann. The OFFICE ACTION of March 22, 2005 states that column 16, lines 2 to 6 teaches the claimed synchronization marker. However, this portion of Mann mentions a synchronization register TSYNC "provided to allow injection of synchronizing address information." Mann states at column 16, lines 13 to 29 (immediately following the portion cited by the Examiner):

> "The processor determines whether each trace record includes address information by, e.g., assuming all TCODES except for TCODE=1 are synchronizing events providing address information. Thus, in the described embodiment, each trace entry having a TCODE not equal to "1" causes a counter to be loaded to the value in the TSYNC register which allows the counter to count the desired maximum number of trace records generated before current program address information is provided. Thus, depending on if the counter is configured as an up counter or down counter, the counter is either loaded with zero or the maximum count, respectively. The counter counts each trace record produced which does not include address information. When the count of such trace records reaches the predetermined number; trace logic provides the current program address as a trace entry, thereby providing said trace synchronization information."

Thus the synchronization register TSYNC causes periodic "providing said trace synchronization information" "(W)hen the count of such trace records reaches the predetermined number." The FINAL REJECTION cites various entries in Table 6 which transmit address

values. If this synchronization register TSYNC produced the synchronization marker recited in claim 1, the entries in Table 6 which transmit address values would transmit an offset value. The FINAL REJECTION fails to point out where Mann teaches these address values are specified "as an offset which indicates a number of program counter values in the program counter trace stream by which said corresponding program counter value is offset from said synchronization marker in said program counter trace stream." As pointed out above the only offset taught in Mann is relative to the segment register. There is no teaching in Mann that a full count in the synchronization register TSYNC (which the FINAL REJECTION alleges corresponds to the recited synchronization marker) causes generation of a new segment address, only that "trace logic provides the current program address as a trace entry." Further there is no teaching in Mann that the addresses provided by the other entries in Table 6 are specified as an offset to a synchronization marker as recited in claim 1. Thus claim 1 is allowable over Mann.

The ADVISORY ACTION states:

> "Applicant has argued against the prior art to go around the prior art, however the claims as recited do not contain the elements as argued. For example, on Pg. 10 applicant argues 'There is no teaching in Mann that a full count in the synchronization register TSYNCH causes generation of a new segment address.' (Examiner disagrees - See comments below for remarks on Pg. 9). The limitation relating to 'full count in the TSYNCH register' is not recited in the claim 1 rejection."

This statement misunderstands the Applicant's argument. The FINAL REJECTION cited operation of the synchronization register TSYNCH causes generation of the claimed synchronization marker. For that to be true, then following trace outputs that specify addresses must be indicated by "a number of program counter values in the program counter trace stream by which said corresponding program

counter value is offset from said synchronization marker in said program counter trace stream." The Applicants urge that the only teaching of indication of such an offset is an offset relative to a segment register. Thus for the operation of the synchronization register TSYNCH to anticipate the claimed synchronization marked, a new segment address must be generated. Since Mann fails to teach this, the operation of the synchronization register TSYNCH fails to anticipate the claimed synchronization marker. The other remarks in the ADVISORY ACTION are similar in that they take issue with a single link in a chain of the Applicants' arguments. The Applicants arguments show that if the Examiner's characterization of Mann is accepted, this leads to contradictions between the teachings of Mann and the recitations of claim 1.

These convolved argument are necessary because the FINAL REJECTION fails to point out with particularly any portion of Mann teaching the recited "expressing said corresponding program counter value as an offset which indicates a number of program counter values in the program counter trace stream by which said corresponding program counter value is offset from said synchronization marker in said program counter trace stream." The Applicants presented this argument to counter a possible interpretation of the Examiner's statements. This would be unnecessary if the Examiner had pointed out where Mann anticipates this "offset" limitation. The Applicants believe the Examiner has not stated where Mann anticipates this limitation because no such teaching exists in Mann. Accordingly, claim 1 is allowable over Mann.

Claim 4 recites subject matter not anticipated by Mann. Claim 4 recites "counting detected occurrences of program counter loads." Mann states at column 16, lines 35 to 55 (including the portion cited in the FINAL REJECTION):

"Referring to FIG. 7, in operation, a counter 701 is set to the value contained in the synchronization register TSYNC 703 whenever a synchronizing trace entry (e.g., containing a branch target address) is generated. Trace control logic 218 determines when a synchronizing trace entry is generated and provides load signal 705 whenever such addresses are generated. This can be summarized as follows. The counter is decremented by one for each TCODE=1, thus providing for a maximum number of consecutive conditional branch instructions.

"Thus, counter 701 is reloaded each time a target address is generated or other appropriate TCODE is generated indicating a synchronizing record has been provided. Counter 701 is decremented by one for trace entries not having an address. If the counter reaches zero, an indication 707 is asserted by counter 701 and provided to trace control 218. In response, trace control 218 causes a trace entry to be inserted with a code indicating that it is a synchronization entry (TCODE=0110) and a current program address. The current program address can be, e.g., the most recently retired instruction."

This portion of Mann teaches that the value loaded into the counter 701 is "the value contained in the synchronization register TSYNC 703." This portion of Mann further teaches the value in counter 701 "is decremented by one for trace entries not having an address." Thus counter 701 is loaded when a program counter load causing a program counter discontinuity occurs. However, counter 701 thereafter counts down for continuous program counter operation, i.e. trace entries "not having an address." Thus the value of counter 701 cannot be the number of program counter loads. Note further that counter 701 is loaded with the value of the synchronization register TSYNC 703 not only upon program counter loads ("each time a target address is generated") but also upon "other appropriate TCODE is generated indicating a synchronizing record has been provided." Thus counter 701 does not store a number of program counter loads and is loaded with the synchronization register TSYNC 703 value upon other conditions in addition to program counter loads. Accordingly, claim 4 is allowable over Mann.

Claim 5 recites subject matter not anticipated by Mann. Claim 5 recites "maintaining a running count of a number of program counter loads that have occurred since insertion of the synchronization marker." Such a count requires a counter to be zeroed upon each synchronization marker and incremented upon each detection of a program counter load. The application teaches this at page 30, lines 13 to 18. Mann teaches that counter 701 is loaded with the synchronization register TSYNC 703 value each time a target address is generated. This occurs upon a program counter load and other conditions. The counter 701 is then decremented on execution of instructions not requiring a new trace address. Thus counter 701 clearly cannot hold the running count recited in claim 5. Accordingly, claim 5 is allowable over Mann.

(2) Claims 13, 15 and 16 were rejected under 35 U.S.C. 103(a) as made obvious by the combination of Sites, U.S. Patent No. 5,764,885, and Mann, U.S. Patent No. 6,009,270.

Claim 13 recites subject matter not made obvious by the combination of Sites and Mann. Claim 13 recites "said program counter identifier operable for expressing said corresponding program counter value as an offset which indicates a number of program counter values in the program counter trace stream by which said corresponding program counter value is offset from said synchronization marker in said program counter trace stream." The OFFICE ACTION cites the same portions of Mann as cited against claim 1 as teaching this limitation. Mann likewise fails to teach the synchronization marker or the offset recited in claim 13. Mann teaches that the trace address values are an offset with a segment base address. Mann includes no teaching that a synchronization marker is the same as the segment base address. Mann teaches providing a new synchronization marker following a taken conditional branch but fails to teach that the trace address values

following such a synchronization marker are offset from the synchronization marker value. Instead, Mann teaches that the trace address values are offset from the prior and still unchanged segment base address. The FINAL REJECTION does not allege that Sites adds any teaching to Mann to make obvious this limitation. Accordingly, claim 13 is allowable over the combination of Sites and Mann.

Claim 15 recites subject matter not made obvious by the combination of Sites and Mann. Claim 15 recites "counting detected occurrences of program counter loads." The FINAL REJECTION cites the same portions of Mann as cited against claim 4 as teaching this limitation. Mann teaches that the value loaded into the counter 701 is "the value contained in the synchronization register TSYNC 703" and that the value in counter 701 "is decremented by one for trace entries not having an address." Thus the value of counter 701 cannot be the number of program counter loads. Note further that counter 701 is loaded with the value of the synchronization register TSYNC 703 not only upon program counter loads ("each time a target address is generated") but also upon "other appropriate TCODE is generated indicating a synchronizing record has been provided." Thus counter 701 does not store a number of program counter loads and is loaded with the synchronization register TSYNC 703 value upon other conditions in addition to program counter loads. The FINAL REJECTION does not allege that Sites adds any teaching to Mann to make obvious this limitation. Accordingly, claim 15 is allowable over the combination of Sites and Mann.

Claim 16 recites subject matter not made obvious by the combination of Sites and Mann. Claim 16 recites "maintaining a running count of a number of program counter loads that have occurred since insertion of the synchronization marker." Such a count requires a counter to be zeroed upon each synchronization marker and incremented upon each detection of a program counter

load. The application teaches this at page 30, lines 13 to 18. The FINAL REJECTION cites the same portions of Mann as cited against claim 5 as teaching this limitation. Mann teaches that counter 701 is loaded with the synchronization register TSYNC 703 value each time a target address is generated. This occurs upon a program counter load and other conditions. The counter 701 is then decremented on execution of instructions not requiring a new trace address. Thus counter 701 clearly cannot hold the running count recited in claim 16. The FINAL REJECTION does not allege that Sites adds any teaching to Mann to make obvious this limitation. Accordingly, claim 16 is allowable over the combination of Sites and Mann.

(3) Claims 23 to 26 were rejected under 35 U.S.C. 103(a) as made obvious by the combination of Sites, U.S. Patent No. 5,764,885, Mann, U.S. Patent No. 6,009,270, and Edwards, U.S. Patent No. 6,732,307.

Claims 23 and 24 recite subject matter not made obvious by the combination of Sites, Mann and Edwards. Claims 23 and 24 recite "said program counter identifier operable for expressing said corresponding program counter value as an offset which indicates a number of program counter values in the program counter trace stream by which said corresponding program counter value is offset from said synchronization marker in said program counter trace stream." The FINAL REJECTION cites the same portions of Mann as cited against claim 13 as teaching this limitation. Mann likewise fails to teach the synchronization marker or the offset recited in claims 23 and 24. Mann teaches that the trace address values are an offset with a segment base address. Mann includes no teaching that a synchronization marker is the same as the segment base address. Mann teaches providing a new synchronization marker following a taken conditional branch but fails to teach that the

trace address values following such a synchronization marker are offset from the synchronization marker value. Instead, Mann teaches that the trace address values are offset from the prior and still unchanged segment base address. The FINAL REJECTION does not allege that Sites or Edwards adds any teaching to Mann to make obvious this limitation. Accordingly, claims 23 and 24 are allowable over the combination of Sites, Mann and Edwards.

Claims 27 and 29 recite subject matter of the same scope as claim 15 except dependent upon respective claims 23 and 24. Claims 27 and 29 are likewise allowable.

Claims 28 and 30 recite subject matter of the same scope as claim 16 except dependent upon respective claims 23 and 24. Claims 28 and 30 are likewise allowable.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

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Respectfully submitted,

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APPENDIX

CLAIMS ON APPEAL

1. A method of providing data processor emulation information, comprising:

providing a program counter trace stream of program counter values used by a data processor;

inserting a synchronization marker into the program counter trace stream; and

providing trace information indicative of each data processing operation performed by the data processor, including identifying a program counter value that corresponds to the data processing operation, said identifying step including expressing said corresponding program counter value as an offset which indicates a number of program counter values in the program counter trace stream by which said corresponding program counter value is offset from said synchronization marker in said program counter trace stream.

4. The method of Claim 1, wherein:

said identifying step includes detecting occurrences of program counter loads in the data processor; and

said identifying step includes counting detected occurrences of program counter loads.

5. The method of Claim 4, wherein said identifying step includes maintaining a running count of a number of program counter loads that have occurred since insertion of the synchronization marker.

13. An apparatus for providing data processor emulation information, comprising:

first and second inputs for coupling to a data processor;

a trace stream generator coupled to said first input for providing a program counter trace stream of program counter values used by the data processor, said trace stream generator operable for inserting a synchronization marker into the program counter trace stream; and

a trace apparatus coupled to said second input for providing trace information indicative of each data processing operation performed by the data processor, including a program counter identifier for identifying a program counter value that corresponds to said data processing operation, said program counter identifier operable for expressing said corresponding program counter value as an offset which indicates a number of program counter values in the program counter trace stream by which said corresponding program counter value is offset from said synchronization marker in said program counter trace stream.

15. The apparatus of Claim 13, wherein:

said program counter identifier is responsive to information received from the data processor for detecting occurrences of program counter loads in the data processor; and

said program counter identifier includes a counter for counting detected occurrences of program counter loads.

16. The apparatus of Claim 15, wherein said counter is operable for maintaining a running count of a number of program counter loads that have occurred since insertion of the synchronization marker.

23. An integrated circuit, comprising:

a data processor for performing a data processing operation; and

an apparatus coupled to said data processor for providing emulation information about said data processing operation, including a trace stream generator for providing a program counter trace stream of program counter values used by said data processor, said trace stream generator operable for inserting a synchronization marker into the program counter trace stream, and a trace apparatus for providing trace information indicative of said data processing operation, said trace apparatus including a program counter identifier for identifying a program counter value that corresponds to said data processing operation, said program counter identifier operable for expressing said corresponding program counter value as an offset which indicates a number of program counter values in the program counter trace stream by which said corresponding program counter value is offset from said synchronization marker in said program counter trace stream.

24. A data processing system, comprising:

an integrated circuit, including a data processor for performing a data processing operation;

an emulation controller coupled to said integrated circuit for controlling emulation operations of said data processor; and

said integrated circuit including an apparatus coupled between said data processor and said emulation controller for providing emulation information about said data processing operation, said apparatus including a trace stream generator for providing a program counter trace stream of program counter values used by said data processor, said trace stream generator operable for inserting a synchronization marker into the program counter trace stream, and said apparatus further including a trace apparatus for providing trace information indicative of said data processing operation, said trace apparatus including a program counter identifier for identifying a program counter value that corresponds to said data

processing operation, said program counter identifier operable for expressing said corresponding program counter value as an offset which indicates a number of program counter values in the program counter trace stream by which said corresponding program counter value is offset from said synchronization marker in said program counter trace stream.

27. The integrated circuit of Claim 23, wherein:

said program counter identifier is responsive to information received from the data processor for detecting occurrences of program counter loads in the data processor; and

said program counter identifier includes a counter for counting detected occurrences of program counter loads.

28. The integrated circuit of Claim 27, wherein:

said counter is operable for maintaining a running count of a number of program counter loads that have occurred since insertion of the synchronization marker.

29. The data processing system of Claim 24, wherein:

said program counter identifier is responsive to information received from the data processor for detecting occurrences of program counter loads in the data processor; and

said program counter identifier includes a counter for counting detected occurrences of program counter loads.

30. The data processing system of Claim 29, wherein:

said counter is operable for maintaining a running count of a number of program counter loads that have occurred since insertion of the synchronization marker.